	Type	Hits	Search Text	DBs	Time Stamp
1	BRS	0	packet and hypercube and classifier	USPAT; USOCR; EPO; JPO; Derwent	2000/09/29 19:36
2	BRS	233	packet and hypercube	USPAT; USOCR; EPO; JPO; Derwent	2000/09/29 19:36
3	BRS	9	packet and hypercube and breakpoint	USPAT; USOCR; EPO; JPO; Derwent	2000/09/29 19:32

	Comments	Error Definition	Errors
1			0
2			0
3		The search/retrieval could not be aborted because it is not currently pending. The search/retrieval could not be aborted because it is not currently pending. The search/retrieval could not be aborted because it is not currently pending.	3

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☒	☐	US 5339396 A	19940816	22	Parallel computer interconnection path selection - comparing next priority coordinate of first selected processing element with correspondin g next priority coordinate of second coordinate set, and sequentially transferring data packet to next coordinate transforming crossbar	
2	☒	☐	US 5367636 A	19941122		switch Interconnected node hypercube network for parallel data processing system - has message decoder and routing logic, with identification numbers of two processors connected to each other through port number n, and varying only in nth bit	
3	☒	☐	US 4814980 A	19890321		Concurrent hypercube system with improved message passing	

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1			IN	☐	☐	☐	☐	☐	☐	☐
2			IN	☐	☐	☐	☐	☐	☐	☐
3			PETERSON, JOHN C , TUAZON, JESUS O , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
4	☒	☐	US 5367636 A	19941122		Hypercube processor network in which the processor indentification numbers of two processors connected to each other through port number n, vary only in the nth bit	
5	☒	☐	US 4729095 A	19880301		Broadcast instruction for use in a high performance computer system	712/203
6	☒	☐	US 4805173 A	19890214		Error control method and apparatus	714/765
7	☒	☐	US 4811210 A	19890307		A plurality of optical crossbar switches and exchange switches for parallel processor computer	710/132
8	☒	☐	US 4814980 A	19890321		Concurrent hypercube system with improved message passing	709/216
9	☒	☐	US 4814973 A	19890321		Parallel processor	712/16 ;
10	☒	☐	US 4870568 A	19890926		Method for searching a database system including parallel processors	707/5
11	☒	☐	US 4933936 A	19900612		Distributed computing system with dual independent communications paths between computers and employing split tokens	370/406
12	☒	☐	US 4933933 A	19900612		Torus routing chip	370/406

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
4			COLLEY, STEPHEN R , KENOYER, STANLEY P , et al.	☐	☐	☐	☐	☐	☐	☐
5			Colley, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
6	714/772		Hillis, W. Daniel , et al.	☐	☐	☐	☐	☐	☐	☐
7	385/17 ; 708/816		McAulay, Alastair D.	☐	☐	☐	☐	☐	☐	☐
8	709/234 ; 709/250 ; 712/12		Peterson, John C. , et al.	☐	☐	☐	☐	☐	☐	☐
9			Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐
10	707/533		Kahle, Brewster , et al.	☐	☐	☐	☐	☐	☐	☐
11	340/825.5 ; 370/432		Rasmussen, Robert D. , et al.	☐	☐	☐	☐	☐	☐	☐
12			Dally, William J. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
13	☒	☐	US 4953930 A	19900904		CPU socket supporting socket-to-socket optical communications	359/118
14	☒	☐	US 4984235 A	19910108		Method and apparatus for routing message packets and recording the roofing sequence	370/392
15	☒	☐	US 5008882 A	19910416		Method and apparatus for eliminating unsuccessful tries in a search tree	370/406
16	☒	☐	US 5010477 A	19910423		Method and apparatus for transferring vector data between parallel processing system with registers & logic for inter-processor data communication independents of processing operations	712/4
17	☒	☐	US 5050096 A	19910917		Path cost computing neural network	706/19
18	☒	☐	US 5050069 A	19910917		Method and apparatus for simulating m-dimension connection networks in and n-dimension network where m is less than n	703/13
19	☒	☐	US 5083265 A	19920121		Bulk-synchronous parallel computer	712/21

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
13	359/154 ; 385/147		Ramsey, Bernard , et al.	☐	☐	☐	☐	☐	☐	☐
14			Hillis, W. Daniel , et al.	☐	☐	☐	☐	☐	☐	☐
15	370/408		Peterson, John C. , et al.	☐	☐	☐	☐	☐	☐	☐
16			Omoda, Koichiro , et al.	☐	☐	☐	☐	☐	☐	☐
17	706/29		Seidman, Abraham N.	☐	☐	☐	☐	☐	☐	☐
18			Hillis, W. Daniel , et al.	☐	☐	☐	☐	☐	☐	☐
19			Valiant, Leslie G.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
20	☒	☐	US 5099235 A	19920324		Method for transferring data through a network of intelligent control stations using decentralized control techniques	340/826
21	☒	☐	US 5105424 A	19920414		Inter-computer message routing system with each computer having separate routinng automata for each dimension of the network	709/243
22	☒	☐	US 5111198 A	19920505		Method of routing a plurality of messages in a multi-node computer network	340/825.52
23	☒	☐	US 5113523 A	19920512		High performance computer system	712/12
24	☒	☐	US 5117420 A	19920526		Method and apparatus for routing message packets	370/400
25	☒	☐	US 5129077 A	19920707		System for partitioning a massively parallel computer	712/13
26	☒	☐	US 5148547 A	19920915		Method and apparatus for interfacing bit-serial parallel processors to a coprocessor	712/22
27	☒	☐	US 5161156 A	19921103		Multiprocessing packet switching connection system having provision for error correction and recovery	714/4
28	☒	☐	US 5163131 A	19921110		Parallel I/O network file server architecture	709/202

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
20	340/825.02 ; 340/827 ; 455/13.1 ; 709/243 ; 709/245		Crookshanks, Rex J.	☐	☐	☐	☐	☐	☐	☐
21			Flaig, Charles M. , et al.	☐	☐	☐	☐	☐	☐	☐
22	370/393 ; 370/410		Kuszmaul, Bradley C.	☐	☐	☐	☐	☐	☐	☐
23			Colley, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
24			Hillis, W. Daniel , et al.	☐	☐	☐	☐	☐	☐	☐
25			Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐
26			Kahle, Brewster A. , et al.	☐	☐	☐	☐	☐	☐	☐
27	370/218 ; 370/422 ; 714/776		Baum, Richard I. , et al.	☐	☐	☐	☐	☐	☐	☐
28	709/219		Row, Edward J. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
29	☒	☐	US 5166674 A	19921124		Multiprocessing packet switching connection system having provision for error correction and recovery	340/825.07
30	☒	☐	US 5170482 A	19921208		Improved hypercube topology for multiprocessor computer systems	712/12
31	☒	☐	US 5170393 A	19921208		Adaptive routing of messages in parallel and distributed processor systems	370/255
32	☒	☐	US 5175865 A	19921229		Partitioning the processors of a massively parallel single array processor into sub-arrays selectively controlled by host computers	712/13
33	☒	☐	US 5187801 A	19930216		Massively-parallel computer system for generating paths in a binomial lattice	712/22
34	☒	☐	US 5191578 A	19930302		Packet parallel interconnection network	370/418
35	☒	☐	US 5195170 A	19930316		Neural-network dedicated processor for solving assignment problems	706/19
36	☒	☐	US 5212773 A	19930518		Wormhole communications arrangement for massively parallel processor	709/243

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
29	712/13		Baum, Richard I. , et al.	☐	☐	☐	☐	☐	☐	☐
30			Shu, Renben , et al.	☐	☐	☐	☐	☐	☐	☐
31	370/400		Peterson, John C. , et al.	☐	☐	☐	☐	☐	☐	☐
32	710/129 ; 712/22		Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐
33	706/62 ; 712/11		Zenios, Stavros A. , et al.	☐	☐	☐	☐	☐	☐	☐
34	340/825.5 ; 370/369		Lee, Kuo-Chu	☐	☐	☐	☐	☐	☐	☐
35	326/35 ; 706/25 ; 706/33 ; 706/38		Eberhardt, Silvio P.	☐	☐	☐	☐	☐	☐	☐
36	712/15 ; 712/23		Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
37	☒	☐	US 5224100 A	19930629		Routing technique for a hierarchical interprocessor-communication network between massively-parallel processors	370/408
38	☒	☐	US 5247694 A	19930921		System and method for generating communications arrangements for routing data in a massively parallel processing system	712/13
39	☒	☐	US 5247613 A	19930921		Massively parallel processor including transpose arrangement for serially transmitting bits of data words stored in parallel	709/246
40	☒	☐	US 5251131 A	19931005		Classification of data records by comparison of records to a training database using probability weights	704/9
41	☒	☐	US 5255368 A	19931019		Method for selecting data communications paths for routing messages between processors in a parallel processing computer system organized as a hypercube	709/243

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
37	340/825.02		Lee, Sue-Kyoung , et al.	☐	☐	☐	☐	☐	☐	☐
38	712/16		Dahl, E. Denning	☐	☐	☐	☐	☐	☐	☐
39	709/238		Bromley, H. Mark	☐	☐	☐	☐	☐	☐	☐
40			Masand, Brij M. , et al.	☐	☐	☐	☐	☐	☐	☐
41	712/12		Barry, Timothy G.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
42	☒	☐	US 5257266 A	19931026		Computer and communications systems employing universal direct spherics processing architectures	714/4
43	☒	☐	US 5265207 A	19931123		Parallel computer system including arrangement for transferring messages from a source processor to selected ones of a plurality of destination processors and combining responses	712/15
44	☒	☐	US 5274818 A	19931228		System and method for compiling a fine-grained array based source program onto a course-grained hardware	717/5
45	☒	☐	US 5276893 A	19940104		Parallel microprocessor architecture	714/10
46	☒	☐	US 5278986 A	19940111		System and method for compiling a source code supporting data parallel variables	717/6
47	☒	☐	US 5280474 A	19940118		Scalable processor to processor and processor-to-I/O interconnection network and method for parallel processing arrays	370/389

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
42			Maki, Stanley C.	☐	☐	☐	☐	☐	☐	☐
43	370/408 ; 709/243 ; 709/252 ; 712/22		Zak, Robert C. , et al.	☐	☐	☐	☐	☐	☐	☐
44	717/7 ; 717/9		Vasilevsky, Alexander D. , et al.	☐	☐	☐	☐	☐	☐	☐
45	712/33 ;		Savaria, Yvon	☐	☐	☐	☐	☐	☐	☐
46	712/23 ; 717/9		Jourdenais, Karen C. , et al.	☐	☐	☐	☐	☐	☐	☐
47	714/802		Nickolls, John R. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
48	☒	☐	US 5305446 A	19940419		Processing devices with improved addressing capabilities, systems and methods	712/34
49	☒	☐	US 5317735 A	19940531		System for parallel computation with three phase processing in processor tiers in which new instructions trigger execution and forwarding	712/203
50	☒	☐	US 5321813 A	19940614		Reconfigurable, fault tolerant, multistage interconnect network and protocol	714/798
51	☒	☐	US 5333268 A	19940726		Parallel computer system	709/244
52	☒	☐	US 5337395 A	19940809		SPIN: a sequential pipeline neurocomputer	706/42
53	☒	☐	US 5339396 A	19940816		Interconnection network and crossbar switch for the same	710/132
54	☒	☐	US 5347654 A	19940913		System and method for optimizing and generating computer-based code in a parallel processing environment	717/9
55	☒	☐	US 5347450 A	19940913		Message routing in a multiprocessor computer system	709/243

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
48			Leach, Jerald G. , et al.	☐	☐	☐	☐	☐	☐	☐
49	370/406 ; 712/11		Schomberg, Hermann	☐	☐	☐	☐	☐	☐	☐
50	370/244 ; 370/388 ; 370/390 ; 370/422 ; 370/447		McMillen, Robert J. , et al.	☐	☐	☐	☐	☐	☐	☐
51	370/408		Douglas, David C. , et al.	☐	☐	☐	☐	☐	☐	☐
52			Vassiliadis, Stamatis , et al.	☐	☐	☐	☐	☐	☐	☐
53	709/243 ; 712/11		Muramatsu, Akira , et al.	☐	☐	☐	☐	☐	☐	☐
54			Sabot, Gary W. , et al.	☐	☐	☐	☐	☐	☐	☐
55	370/440 ; 709/227		Nugent, Steven F.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
56	☒	☐	US 5353412 A	19941004		Partition control circuit for separately controlling message sending of nodes of tree-shaped routing network to divide the network into a number of partitions	709/243
57	☒	☐	US 5355453 A	19941011		Parallel I/O network file server architecture	709/219
58	☒	☐	US 5355494 A	19941011		Compiler for performing incremental live variable analysis for data-parallel programs	717/6
59	☒	☐	US 5355492 A	19941011		System for compiling parallel communications instructions including their embedded data transfer information	717/7
60	☒	☐	US 5361363 A	19941101		Input/output system for parallel computer for performing parallel file transfers between selected number of input/output devices and another selected number of processing nodes	712/22
61	☒	☐	US 5361334 A	19941101		Data processing and communication	709/243

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
56	340/825.02 ; 370/408 ; 709/252		Douglas, David C. , et al.	☐	☐	☐	☐	☐	☐	☐
57	709/212		Row, Edward J. , et al.	☐	☐	☐	☐	☐	☐	☐
58	717/7 ; 717/9		Sistare, Steven J. , et al.	☐	☐	☐	☐	☐	☐	☐
59	712/22 ; 717/9		Frankel, James L. , et al.	☐	☐	☐	☐	☐	☐	☐
60	712/16		Wells, David , et al.	☐	☐	☐	☐	☐	☐	☐
61	709/234 ; 709/314		Cawley, Robin A.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
62	☒	☐	US 5367692 A	19941122		Parallel computer system including efficient arrangement for performing communications among processing node to effect an array transposition operation	712/22
63	☒	☐	US 5367642 A	19941122		System of express channels in an interconnection network that automatically bypasses local channel addressable nodes	709/253
64	☒	☐	US 5367636 A	19941122		Hypercube processor network in which the processor indentification numbers of two processors connected to each other through port number n, vary only in the nth bit	709/245
65	☒	☐	US 5377182 A	19941227		Non-blocking crossbar permutation engine with constant routing latency	370/219

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
62	712/12		Edelman, Alan S.	☐	☐	☐	☐	☐	☐	☐
63	709/239		Dally, William J.	☐	☐	☐	☐	☐	☐	☐
64	370/400		Colley, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
65	340/825.8 ; 340/827 ; 370/355 ; 370/388 ; 370/400 ; 379/221 ; 379/335		Monacos, Steve P.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
66	☒	☐	US 5379440 A	19950103		Parallel processor with array of clustered processing elements having inputs seperate from outputs and outputs limited to a maximum of two per dimension	712/12
67	☒	☐	US 5381550 A	19950110		System and method for compiling a source code supporting data parallel variables	717/6
68	☒	☐	US 5388214 A	19950207		Parallel computer system including request distribution network for distributing processing requests to selected sets of processors in parallel	712/15
69	☒	☐	US 5390336 A	19950214		C' parallel computer system having processing nodes with distributed memory with memory addresses defining unitary system address space	712/22
70	☒	☐	US 5390304 A	19950214		Method and apparatus for processing block instructions in a data processor	712/241

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
66			Kelly, Thomas , et al.	☐	☐	☐	☐	☐	☐	☐
67			Jourdenais, Karen C. , et al.	☐	☐	☐	☐	☐	☐	☐
68	712/18		Leiserson, Charles E. , et al.	☐	☐	☐	☐	☐	☐	☐
69			Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐
70	710/22 ; 712/36		Leach, Jerald G. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
71	☒	☐	US 5390298 A	19950214		Parallel computer system including arrangement for quickly draining messages from message router	712/22
72	☒	☐	US 5398317 A	19950314		Synchronous message routing using a retransmitted clock signal in a multiprocessor computer system	709/248
73	☒	☐	US 5404562 A	19950404		Massively parallel processor including queue-based message delivery system	712/18
74	☒	☐	US 5404550 A	19950404		Method and apparatus for executing tasks by following a linked list of memory packets	712/14
75	☒	☐	US 5404296 A	19950404		Massively parallel computer arrangement for analyzing seismic data pursuant to pre-stack depth migration methodology	702/14
76	☒	☐	US 5410652 A	19950425		Data communication control by arbitrating for a data transfer control token with facilities for halting a data transfer by maintaining possession of the token	370/450

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
71	370/408 ; 370/409 ; 712/13		Kuszmaul, Bradley C. , et al.	☐	☐	☐	☐	☐	☐	☐
72	340/825.03 ; 710/131		Nugent, Steven F.	☐	☐	☐	☐	☐	☐	☐
73	709/238		Heller, Steven K. , et al.	☐	☐	☐	☐	☐	☐	☐
74			Horst, Robert W.	☐	☐	☐	☐	☐	☐	☐
75	367/72		Moorhead, William D.	☐	☐	☐	☐	☐	☐	☐
76	370/455 ; 370/457 ; 370/462 ; 710/240		Leach, Jerald G. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
77	☒	☐	US 5434972 A	19950718		Network for determining route through nodes by directing searching path signal arriving at one port of node to another port receiving free path signal	709/238
78	☒	☐	US 5444701 A	19950822		Method of packet routing in torus networks with two buffers per edge	370/406
79	☒	☐	US 5446572 A	19950829		Optical interconnects for high speed backplanes using spectral slicing	359/133
80	☒	☐	US 5452468 A	19950919		Computer system with parallel processing for information organization	345/419 ;
81	☒	☐	US 5471623 A	19951128		Lambda network having 2.sup.m-1 nodes in each of m stages with each node coupled to four other nodes for bidirectional routing of data packets between nodes	709/243
82	☒	☐	US 5475857 A	19951212		Express channels for diminishing latency and increasing throughput in an interconnection network	712/11
83	☒	☐	US 5485627 A	19960116		Partitionable massively parallel processing system	712/13

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
77	370/256 ; 370/408 ; 707/10		Hamlin, Derrick J.	☐	☐	☐	☐	☐	☐	☐
78			Cypher, Robert E. , et al.	☐	☐	☐	☐	☐	☐	☐
79	359/124 ; 359/127 ; 359/130		Husbands, Charles R. , et al.	☐	☐	☐	☐	☐	☐	☐
80			Peterson, Richard E.	☐	☐	☐	☐	☐	☐	☐
81	370/412 ; 709/235 ; 709/245 ;		Napolitano, Jr., Leonard M.	☐	☐	☐	☐	☐	☐	☐
82	710/100 ; 710/101 ; 710/126		Dally, William J.	☐	☐	☐	☐	☐	☐	☐
83	710/131		Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
84	☒	☐	US 5511163 A	19960423		Network adaptor connected to a computer for virus signature recognition in all files on a network	714/28
85	☒	☐	US 5515535 A	19960507		System and method for parallel variable optimization	717/6
86	☒	☐	US 5517662 A	19960514		Multiprocessor system with distributed memory	709/201
87	☒	☐	US 5517619 A	19960514		Interconnection network and crossbar switch for the same	709/243
88	☒	☐	US 5522070 A	19960528		Computer resource distributing method and system for distributing a multiplicity of processes to a plurality of computers connected in a network	709/104
89	☒	☐	US 5524212 A	19960604		Multiprocessor system with write generate method for updating cache	711/121
90	☒	☐	US 5530809 A	19960625		Router for parallel computer including arrangement for redirecting messages	709/250
91	☒	☐	US 5535373 A	19960709		Protocol-to-protocol translator for interfacing disparate serial network nodes to a common parallel switching network	703/25

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
84	714/39		Lerche, Michael , et al.	☐	☐	☐	☐	☐	☐	☐
85	717/7 ; 717/9		Frankel, James L. , et al.	☐	☐	☐	☐	☐	☐	☐
86	709/250 ; 710/132 ; 710/39 ; 712/30		Coleman, John J. , et al.	☐	☐	☐	☐	☐	☐	☐
87			Muramatsu, Akira , et al.	☐	☐	☐	☐	☐	☐	☐
88	709/226		Sumimoto, Shinji	☐	☐	☐	☐	☐	☐	☐
89	711/141 ; 711/144		Somani, Arun K. , et al.	☐	☐	☐	☐	☐	☐	☐
90	709/238 ; 709/245		Douglas, David C. , et al.	☐	☐	☐	☐	☐	☐	☐
91	370/466 ; 703/26 ; 703/27		Olnowich, Howard T.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
92	☒	☐	US 5535348 A	19960709		Block instruction	712/241
93	☒	☐	US 5541914 A	19960730		Packet-switched self-routing multistage interconnection network having contention-free fanout, low-loss routing, and fanin buffering to efficiently realize arbitrarily low packet loss	370/427
94	☒	☐	US 5551039 A	19960827		Compiling a source code vector instruction by generating a subgrid loop for iteratively processing array elements by plural processing elements	717/6
95	☒	☐	US 5553068 A	19960903		ATM cell broadcasting system	370/399
96	☒	☐	US 5561805 A	19961001		System for selectively packing together datablocks and efficiently routing independent of network topology in a parallel computer system in accordance with a selected numbering system	709/238
97	☒	☐	US 5561801 A	19961001		System and method for multilevel promotion	717/6
98	☒	☐	US 5574933 A	19961112		Task flow computer architecture	712/28

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
92			Leach, Jerald G. , et al.	☐	☐	☐	☐	☐	☐	☐
93	359/117 ;		Krishnamoorthy, Ashok V. , et al.	☐	☐	☐	☐	☐	☐	☐
94			Weinberg, Tobias M. , et al.	☐	☐	☐	☐	☐	☐	☐
95	370/390		Aso, Yasuhiro , et al.	☐	☐	☐	☐	☐	☐	☐
96	710/38		Bruck, Jehoshua , et al.	☐	☐	☐	☐	☐	☐	☐
97			Simons, Joshua E. , et al.	☐	☐	☐	☐	☐	☐	☐
98	710/30 ; 710/33 ; 710/52		Horst, Robert W.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
99	☒	☐	US 5574849 A	19961112		Synchronized data transmission between elements of a processing system	714/12
100	☒	☐	US 5588152 A	19961224		Advanced parallel processor including advanced support hardware	712/16
101	☒	☐	US 5590345 A	19961231		Advanced parallel array processor(APAP)	712/11
102	☒	☐	US 5590283 A	19961231		Parallel computer system with physically separate tree networks for data and control messages	712/29
103	☒	☐	US 5592610 A	19970107		Method and apparatus for enhancing the fault-tolerance of a network	714/4
104	☒	☐	US 5594918 A	19970114		Parallel computer system providing multi-ported intelligent memory	712/15
105	☒	☐	US 5594914 A	19970114		Method and apparatus for accessing multiple memory devices	712/42
106	☒	☐	US 5594866 A	19970114		Message routing in a multi-processor computer system with alternate edge strobe regeneration	709/234
107	☒	☐	US 5598408 A	19970128		Scalable processor to processor and processor to I/O interconnection network and method for parallel processing arrays	370/351

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
99			Sonnier, David P. , et al.	☐	☐	☐	☐	☐	☐	☐
100			Dapp, Michael C. , et al.	☐	☐	☐	☐	☐	☐	☐
101	712/14 ; 712/15		Barker, Thomas N. , et al.	☐	☐	☐	☐	☐	☐	☐
102	709/243 ; 709/252 ; 710/128		Hillis, W. Daniel , et al.	☐	☐	☐	☐	☐	☐	☐
103	714/43		Chittor, Suresh S.	☐	☐	☐	☐	☐	☐	☐
104	712/13 ; 712/20 ; 714/12		Knowles, Billy J. , et al.	☐	☐	☐	☐	☐	☐	☐
105			Coomes, Joseph A. , et al.	☐	☐	☐	☐	☐	☐	☐
106	370/517 ; 375/211 ; 375/214 ; 709/243		Nugent, Steven F.	☐	☐	☐	☐	☐	☐	☐
107	370/380 ; 370/388 ; 709/238 ; 710/132 ; 712/11		Nickolls, John R. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
108	☒	☐	US 5602839 A	19970211		Adaptive and dynamic message routing system for multinode wormhole networks	370/405
109	☒	☐	US 5603044 A	19970211		Interconnection network for a multi-nodal data processing system which exhibits incremental scalability	710/102
110	☒	☐	US 5608448 A	19970304		Hybrid architecture for video on demand server	348/7
111	☒	☐	US 5611038 A	19970311		Audio/video transceiver provided with a device for reconfiguration of incompatibly received or transmitted video and audio information	345/302
112	☒	☐	US 5612953 A	19970318		Multi-media serial line switching adapter for parallel networks and heterogeneous and homologous computer systems	370/367
113	☒	☐	US 5612897 A	19970318		Symmetrically switched multimedia system	709/219
114	☒	☐	US 5617413 A	19970401		Scalable wrap-around shuffle exchange network with deflection routing	370/400
115	☒	☐	US 5617233 A	19970401		Transparent optical node structure	359/123
116	☒	☐	US 5617577 A	19970401		Advanced parallel array processor I/O connection	712/12

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
108			Annapareddy, Narasimhareddy , et al.	☐	☐	☐	☐	☐	☐	☐
109	361/733 ; 361/788 ; 361/803 ; 436/65 ; 439/61		Annapareddy, Narasimhareddy L. , et al.	☐	☐	☐	☐	☐	☐	☐
110	348/12 ; 348/13		Smoral, Vincent J. , et al.	☐	☐	☐	☐	☐	☐	☐
111	345/327 ; 348/390.1 ; 709/221 ;		Shaw, Venson M. , et al.	☐	☐	☐	☐	☐	☐	☐
112	370/389		Olnowich, Howard T.	☐	☐	☐	☐	☐	☐	☐
113	345/302		Rege, Satish L.	☐	☐	☐	☐	☐	☐	☐
114	370/427		Monacos, Steve P.	☐	☐	☐	☐	☐	☐	☐
115	359/158 ; 370/389		Boncek, Raymond K.	☐	☐	☐	☐	☐	☐	☐
116	712/15 ; 712/20		Barker, Thomas N. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
117	☒	☐	US 5617538 A	19970401		Message transfer system and method for parallel computer with message transfers being scheduled by skew and roll functions to avoid bottlenecks	709/245
118	☒	☐	US 5625836 A	19970429		SIMD/MIMD processing memory element (PME)	709/214
119	☒	☐	US 5630162 A	19970513		Array processor dotted communication network based on H-DOTs	712/20
120	☒	☐	US 5638516 A	19970610		Parallel processor that routes messages around blocked or faulty nodes by selecting an output port to a subsequent node from a port vector and transmitting a route ready signal back to a previous node	709/239
121	☒	☐	US 5659796 A	19970819		System for randomly modifying virtual channel allocation and accepting the random modification based on the cost function	709/241
122	☒	☐	US 5659781 A	19970819		Bidirectional systolic ring network	712/11
123	☒	☐	US 5659778 A	19970819		System and method of mapping an array to processing elements	712/11

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
117	709/216 ; 710/3		Heller, Steven K.	☐	☐	☐	☐	☐	☐	☐
118	711/147 ; 712/201		Barker, Thomas N. , et al.	☐	☐	☐	☐	☐	☐	☐
119	700/2 ; 712/11		Wilkinson, Paul A. , et al.	☐	☐	☐	☐	☐	☐	☐
120	709/229 ; 709/237		Duzett, Robert C. , et al.	☐	☐	☐	☐	☐	☐	☐
121	370/409		Thorson, Gregory M. , et al.	☐	☐	☐	☐	☐	☐	☐
122	712/19 ;		Larson, Noble G.	☐	☐	☐	☐	☐	☐	☐
123			Gingold, David Bruce , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
124	☒	☐	US 5675807 A	19971007		Interrupt message delivery identified by storage location of received interrupt data	710/260
125	☒	☐	US 5675579 A	19971007		Method for verifying responses to messages using a barrier message	370/248
126	☒	☐	US 5680550 A	19971021		Digital computer for determining a combined tag value from tag values selectively incremented and decremented reflecting the number of messages transmitted and not received	712/11
127	☒	☐	US 5682479 A	19971028		System and method for network exploration and access	709/242
128	☒	☐	US 5684807 A	19971104		Adaptive distributed system and method for fault tolerance	714/712
129	☒	☐	US 5689689 A	19971118		Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal	709/400

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
124	710/263 ; 710/268 ; 710/269 ; 710/4 ; 714/48		Iswandhi, Geoffrey I. , et al.	☐	☐	☐	☐	☐	☐	☐
125	370/241 ; 709/237 ; 714/43		Watson, William Joel , et al.	☐	☐	☐	☐	☐	☐	☐
126	712/16 ; 712/20		Kuszmaul, Bradley C. , et al.	☐	☐	☐	☐	☐	☐	☐
127	370/254 ; 370/355 ; 370/403 ; 370/466 ; 709/241		Newhall, Robert E. , et al.	☐	☐	☐	☐	☐	☐	☐
128	714/4		Bianchini, Jr., Ronald P. , et al.	☐	☐	☐	☐	☐	☐	☐
129	713/400 ; 713/500		Meyers, Steven C. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
130	☒	☐	US 5701416 A	19971223		Adaptive routing mechanism for torus interconnection network	712/11
131	☒	☐	US 5708836 A	19980113		SIMD/MIMD inter-processor communication	712/20
132	☒	☐	US 5710935 A	19980120		Advanced parallel array processor (APAP)	712/20
133	☒	☐	US 5710938 A	19980120		Data processing array in which sub-arrays are established and run independently	712/13
134	☒	☐	US 5713037 A	19980127		Slide bus communication functions for SIMD/MIMD array processor	702/33
135	☒	☐	US 5717943 A	19980210		Advanced parallel array processor (APAP)	712/20
136	☒	☐	US 5717944 A	19980210		Autonomous SIMD/MIMD processor memory elements	712/20
137	☒	☐	US 5721819 A	19980224		Programmable, distributed network routing	709/243
138	☒	☐	US 5734826 A	19980331		Variable cyclic redundancy coding method and apparatus for use in a multistage network	709/238
139	☒	☐	US 5734921 A	19980331		Advanced parallel array processor computer package	712/10

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
130	340/825.02 ; 340/825.03 ; 340/826 ; 340/827 ; 709/243 ; 712/2 ; 712/21		Thorson, Gregory M. , et al.	☐	☐	☐	☐	☐	☐	☐
131	712/11 ; 712/14 ; 712/15		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
132	711/149 ; 712/11 ; 712/15		Barker, Thomas Norman , et al.	☐	☐	☐	☐	☐	☐	☐
133	712/15		Dahl, Curtis Wayne , et al.	☐	☐	☐	☐	☐	☐	☐
134	712/14 ; 712/20		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
135	712/14		Barker, Thomas Norman , et al.	☐	☐	☐	☐	☐	☐	☐
136	712/14		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
137	709/242		Galles, Michael B. , et al.	☐	☐	☐	☐	☐	☐	☐
138	370/410 ; 714/52 ; 714/758		Olnowich, Howard Thomas , et al.	☐	☐	☐	☐	☐	☐	☐
139	709/238 ; 712/14 ; 712/20		Dapp, Michael Charles , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
140	☒	☐	US 5740463 A	19980414		Information processing system and method of computation performed with an information processing system	712/11
141	☒	☐	US 5752067 A	19980512		Fully scalable parallel processing system having asynchronous SIMD processing	712/16
142	☒	☐	US 5751991 A	19980512		Processing devices with improved addressing capabilities, systems and methods	711/214
143	☒	☐	US 5751955 A	19980512		Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory	714/12
144	☒	☐	US 5751932 A	19980512		Fail-fast, fail-functional, fault-tolerant multiprocessor system	714/12
145	☒	☐	US 5751710 A	19980512		Technique for connecting cards of a distributed network switch	370/423
146	☒	☐	US 5751454 A	19980512		Wavelength bypassed ring networks	359/119
147	☒	☐	US 5754871 A	19980519		Parallel processing system having asynchronous SIMD processing	712/20

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
140	712/12		Oshima, Takeharu , et al.	☐	☐	☐	☐	☐	☐	☐
141			Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
142	711/220 ; 712/208		Leach, Jerald G. , et al.	☐	☐	☐	☐	☐	☐	☐
143	709/400 ; 712/43 ; 714/11		Sonnier, David Paul , et al.	☐	☐	☐	☐	☐	☐	☐
144			Horst, Robert W. , et al.	☐	☐	☐	☐	☐	☐	☐
145	370/427 ; 370/536 ; 710/131		Crowther, William R. , et al.	☐	☐	☐	☐	☐	☐	☐
146	359/110 ; 359/128 ; 370/222		MacDonald, R. Ian , et al.	☐	☐	☐	☐	☐	☐	☐
147	712/11 ; 712/229		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
148	☒	☐	US 5761721 A	19980602		Method and system for cache coherence despite unordered interconnect transport	711/141
149	☒	☐	US 5761523 A	19980602		Parallel processing system having asynchronous SIMD processing and data parallel coding	712/20
150	☒	☐	US 5765015 A	19980609		Slide network for an array processor	712/22
151	☒	☐	US 5765012 A	19980609		Controller for a SIMD/MIMD array having an instruction sequencer utilizing a canned routine library	712/16
152	☒	☐	US 5765011 A	19980609		Parallel processing system having a synchronous SIMD processing with processing elements emulating SIMD operation using individual instruction streams	712/20
153	☒	☐	US 5774698 A	19980630		Multi-media serial line switching adapter for parallel networks and heterogeneous and homologous computer system	712/1

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
148	711/118 ; 711/124 ; 711/154 ; 711/210		Baldus, Donald Francis , et al.	☐	☐	☐	☐	☐	☐	☐
149	712/203		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
150	709/238 ; 712/11		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
151	712/245		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
152	712/203		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
153	370/366		Olnowich, Howard Thomas	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
154	☒	☐	US 5790776 A	19980804		Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements	714/10
155	☒	☐	US 5794059 A	19980811		N-dimensional modified hypercube	712/10
156	☒	☐	US 5802366 A	19980901		Parallel I/O network file server architecture	709/250
157	☒	☐	US 5805915 A	19980908		SIMIMD array processing system	712/20
158	☒	☐	US 5809309 A	19980915		Processing devices with look-ahead instruction systems and methods	710/260
159	☒	☐	US 5809292 A	19980915		Floating point for simid array machine	712/222
160	☒	☐	US 5815723 A	19980929		Picket autonomy on a SIMD machine	712/20
161	☒	☐	US 5822381 A	19981013		Distributed global clock system	375/356
162	☒	☐	US 5821986 A	19981013		Method and apparatus for visual communications in a scalable network environment	348/17
163	☒	☐	US 5826101 A	19981020		Data processing device having split-mode DMA channel	712/34

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
154	710/18 ; 710/32 ; 710/61 ; 714/12		Sonnier, David Paul , et al.	☐	☐	☐	☐	☐	☐	☐
155	712/1 ; 712/11 ; 712/12 ; 712/13 ; 712/15		Barker, Thomas Norman , et al.	☐	☐	☐	☐	☐	☐	☐
156			Row, Edward John , et al.	☐	☐	☐	☐	☐	☐	☐
157	712/16 ; 712/22		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
158	712/233		Leach, Jerald G. , et al.	☐	☐	☐	☐	☐	☐	☐
159	708/496 ; 708/513 ; 708/550 ; 712/14 ; 712/22 ; 712/300		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
160	712/13 ; 712/14		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
161	375/358 ; 375/371		Parry, David M. , et al.	☐	☐	☐	☐	☐	☐	☐
162	348/15 ; 379/93.21		Yuan, Xiancheng , et al.	☐	☐	☐	☐	☐	☐	☐
163	710/22		Beck, Michael D. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
164	☒	☐	US 5828894 A	19981027		Array processor having grouping of SIMD pickets	712/20
165	☒	☐	US 5832295 A	19981103		System for detecting the presence or absence of a loss of transfer word by checking reception side judgement bits	710/1
166	☒	☐	US 5838894 A	19981117		Logical, fail-functional, dual central processor units formed from three processor units	714/11
167	☒	☐	US 5842031 A	19981124		Advanced parallel array processor (APAP)	712/23
168	☒	☐	US 5862403 A	19990119		Continuous data server apparatus and data transfer scheme enabling multiple simultaneous data accesses	710/6
169	☒	☐	US 5867501 A	19990202		Encoding for communicating data and commands	370/474
170	☒	☐	US 5867727 A	19990202		System for judging read out transfer word is correct by comparing flag of transfer word and lower bit portion of read destination selection address	710/4
171	☒	☐	US 5870619 A	19990209		Array processor with asynchronous availability of a next SIMD instruction	712/20

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
164	712/13 ; 712/14		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
165	714/758		Hattori, Hiroshi	☐	☐	☐	☐	☐	☐	☐
166	709/239 ; 714/12		Horst, Robert W.	☐	☐	☐	☐	☐	☐	☐
167			Barker, Thomas Norman , et al.	☐	☐	☐	☐	☐	☐	☐
168			Kanai, Tatsunori , et al.	☐	☐	☐	☐	☐	☐	☐
169			Horst, Robert W. , et al.	☐	☐	☐	☐	☐	☐	☐
170			Hattori, Hiroshi	☐	☐	☐	☐	☐	☐	☐
171	712/203		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
172	☒	☐	US 5875475 A	19990223		Continuous data server apparatus and method for controlling continuous data server	711/154
173	☒	☐	US 5875190 A	19990223		Asynchronous transfer mode switching system	370/395
174	☒	☐	US 5878241 A	19990302		Partitioning of processing elements in a SIMD/MIMD array processor	712/203
175	☒	☐	US 5878227 A	19990302		System for performing deadlock free message transfer in cyclic multi-hop digital computer network using a number of buffers based on predetermined diameter	709/235
176	☒	☐	US 5881304 A	19990309		Incidence graph based communications and operations method and apparatus for parallel processing architecture	712/11
177	☒	☐	US 5884046 A	19990316		Apparatus and method for sharing data and routing messages between a plurality of workstations in a local area network	709/238

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
172	348/7 ; 711/114		Kizu, Toshiki , et al.	☐	☐	☐	☐	☐	☐	☐
173	370/423 ; 370/434 ; 370/458 ;		Law, Ka Lun	☐	☐	☐	☐	☐	☐	☐
174	712/20		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
175	370/229 ; 709/238		Wade, Jon P. , et al.	☐	☐	☐	☐	☐	☐	☐
176			Rolfe, David B. , et al.	☐	☐	☐	☐	☐	☐	☐
177	709/202 ; 709/203 ; 709/219 ; 709/239 ; 709/251 ; 709/252		Antonov, Vadim	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
178	☒	☐	US 5898826 A	19990427		Method and apparatus for deadlock-free routing around an unusable routing component in an N-dimensional network	714/4
179	☒	☐	US 5897657 A	19990427		Multiprocessing system employing a coherency protocol including a reply count	711/145
180	☒	☐	US 5901328 A	19990504		System for transferring data between main computer multiport memory and external device in parallel system utilizing memory protection scheme and changing memory protection area	710/5
181	☒	☐	US 5903770 A	19990511		Incidence graph based communications and operations method and apparatus for parallel processing architecture	712/11
182	☒	☐	US 5903673 A	19990511		Digital video signal encoder and encoding method	382/236
183	☒	☐	US 5912893 A	19990615		Incidence graph based communications and operations method and apparatus for parallel processing architecture	370/406

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
178			Pierce, Paul R. , et al.	☐	☐	☐	☐	☐	☐	☐
179	711/148		Hagersten, Erik E. , et al.	☐	☐	☐	☐	☐	☐	☐
180	711/100 ; 711/147 ; 711/149 ; 711/152		Ooe, Kazuichi	☐	☐	☐	☐	☐	☐	☐
181			Rolfe, David B. , et al.	☐	☐	☐	☐	☐	☐	☐
182	382/239		Wang, Albert S. , et al.	☐	☐	☐	☐	☐	☐	☐
183	700/4 ; 709/213 ; 709/238		Rolfe, David B. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
184	☒	☐	US 5913069 A	19990615		Interleaving memory in distributed vector architecture multiprocessor system	712/2
185	☒	☐	US 5913070 A	19990615		Inter-connector for use with a partitionable massively parallel processing system	712/13
186	☒	☐	US 5914953 A	19990622		Network message routing using routing table information and supplemental enable information for deadlock prevention	370/392
187	☒	☐	US 5928332 A	19990727		Communication network with reversible source routing that includes reduced header information being calculated in accordance with an equation	709/242
188	☒	☐	US 5931918 A	19990803		Parallel I/O network file server architecture	709/321
189	☒	☐	US 5937202 A	19990810		High-speed, parallel, processor architecture for front-end electronics, based on a single type of ASIC, and method use thereof	712/19

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
184	711/157		Sugumar, Rabin A. , et al.	☐	☐	☐	☐	☐	☐	☐
185			Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐
186	370/389 ; 709/238		Krause, John C. , et al.	☐	☐	☐	☐	☐	☐	☐
187	709/238		Pierce, Paul R.	☐	☐	☐	☐	☐	☐	☐
188			Row, Edward John , et al.	☐	☐	☐	☐	☐	☐	☐
189	712/11		Crosetto, Dario B.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
190	☒	☐	US 5938765 A	19990817		System and method for initializing a multinode multiprocessor computer system	713/1
191	☒	☐	US 5940367 A	19990817		Fault-tolerant butterfly switch	370/218
192	☒	☐	US 5941969 A	19990824		Bridge for direct data storage device access	710/128
193	☒	☐	US 5946496 A	19990831		Distributed vector architecture	712/2
194	☒	☐	US 5963746 A	19991005		Fully distributed processing memory element	712/20
195	☒	☐	US 5963745 A	19991005		APAP I/O programmable router	712/13
196	☒	☐	US 5966528 A	19991012		SIMD/MIMD array processor with vector processing	712/222
197	☒	☐	US 5964835 A	19991012		Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source	709/216
198	☒	☐	US 5970232 A	19991019		Router table lookup mechanism	709/238

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
190	713/100 ; 713/2		Dove, Kenneth Frank , et al.	☐	☐	☐	☐	☐	☐	☐
191	340/827 ; 370/224 ; 370/225 ; 370/236 ; 370/389 ; 370/404 ; 370/427		Antonov, Vadim	☐	☐	☐	☐	☐	☐	☐
192	709/212		Ram, Tamir , et al.	☐	☐	☐	☐	☐	☐	☐
193	711/157 ; 712/219		Sugumar, Rabin A. , et al.	☐	☐	☐	☐	☐	☐	☐
194	709/238 ; 712/14		Barker, Thomas Norman , et al.	☐	☐	☐	☐	☐	☐	☐
195	712/10 ; 712/12 ; 712/14		Collins, Clive Allan , et al.	☐	☐	☐	☐	☐	☐	☐
196	712/10 ; 712/203 ; 712/229		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
197	711/152 ; 711/163		Fowler, Daniel L. , et al.	☐	☐	☐	☐	☐	☐	☐
198	370/351 ; 370/389 ; 712/13		Passint, Randal S. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
199	☒	☐	US 5974456 A	19991026		System and method for input/output flow control in a multiprocessor computer system	709/223
200	☒	☐	US 5978570 A	19991102		Memory system providing page mode memory access arrangement	711/200
201	☒	☐	US 5991866 A	19991123		Method and system for generating a program to facilitate rearrangement of address bits among addresses in a massively parallel processor system	712/10
202	☒	☐	US 5996020 A	19991130		Multiple level minimum logic network	709/238
203	☒	☐	US 6006255 A	19991221		Networked computer system and method of communicating using multiple request packet classes to prevent deadlock	709/216
204	☒	☐	US 6014690 A	20000111		Employing multiple channels for deadlock avoidance in a cache coherency protocol	709/215
205	☒	☐	US 6016510 A	20000118		TORUS routing element error handling and self-clearing with programmable watermarking	709/233
206	☒	☐	US 6016469 A	20000118		Process for the vector quantization of low bit rate vocoders	704/222

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
199	710/39 ; 710/6		Naghshineh, Kianoosh , et al.	☐	☐	☐	☐	☐	☐	☐
200			Hillis, W. Daniel	☐	☐	☐	☐	☐	☐	☐
201	712/12 ; 712/14 ; 712/16		Heller, Steven K. , et al.	☐	☐	☐	☐	☐	☐	☐
202	709/239 ; 709/240		Reed, Coke S.	☐	☐	☐	☐	☐	☐	☐
203			Hoover, Russell Dean , et al.	☐	☐	☐	☐	☐	☐	☐
204	709/201 ; 709/214 ; 709/400		VanDoren, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
205			Quattromani, Marc Alan , et al.	☐	☐	☐	☐	☐	☐	☐
206	704/230		Laurent, Pierre Andre	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
207	☒	☐	US 6016211 A	20000118		Optoelectronic smart pixel array for a reconfigurable intelligent optical interconnect	359/117
208	☒	☐	US 6016307 A	20000118		Multi-protocol telecommunications routing optimization	370/238
209	☒	☐	US 6021118 A	20000201		Synchronization methods for distributed processing systems having replicated data	370/254
210	☒	☐	US 6026444 A	20000215		TORUS routing element error handling and self-clearing with link lockup prevention	709/232
211	☒	☐	US 6028541 A	20000222		Lossless data compression with low complexity	341/76

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
207	359/108 ; 359/163 ; 708/191 ;		Szymanski, Ted , et al.	☐	☐	☐	☐	☐	☐	☐
208	370/243 ; 370/252		Kaplan, Allen D. , et al.	☐	☐	☐	☐	☐	☐	☐
209	370/503		Houck, David J. , et al.	☐	☐	☐	☐	☐	☐	☐
210	370/229 ; 370/235 ; 370/236 ; 709/231 ; 709/233 ; 709/235 ; 709/238 ; 709/243 ; 710/125 ; 710/29 ; 710/33 ; 710/34 ; 710/52 ; 714/51 ; 714/54		Quattromani, Marc Alan , et al.	☐	☐	☐	☐	☐	☐	☐
211	341/50		Levine, Earl	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
212	☒	☐	US 6041358 A	20000321		Method for maintaining virtual local area networks with mobile terminals in an ATM network	709/238
213	☒	☐	US 6044080 A	20000328		Scalable parallel packet router	370/401
214	☒	☐	US 6043763 A	20000328		Lossless data compression with low complexity	341/51
215	☒	☐	US 6055618 A	20000425		Virtual maintenance network in multiprocessing system having a non-flow controlled virtual maintenance channel	712/11
216	☒	☐	US 6081883 A	20000627		Processing system with dynamically allocatable buffer memory	712/28
217	☒	☐	US 6085303 A	20000704		Seralized race-free virtual barrier network	712/16
218	☒	☐	US 6085276 A	20000704		Multi-processor computer system having a data switch with simultaneous insertion buffers for eliminating arbitration interdependencies	710/240
219	☒	☐	US 6088770 A	20000711		Shared memory multiprocessor performing cache coherency	711/148

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
212	370/331 ; 370/397 ; 379/88.19 ; 455/461 ; 709/215 ; 709/223 ; 709/228 ; 709/239 ; 709/243 ; 709/249		Huang, Nen-Fu , et al.	☐	☐	☐	☐	☐	☐	☐
213	370/235		Antonov, Vadim	☐	☐	☐	☐	☐	☐	☐
214	341/106		Levine, Earl	☐	☐	☐	☐	☐	☐	☐
215	370/254 ; 370/406 ; 370/409 ; 709/240 ; 712/28		Thorson, Gregory M.	☐	☐	☐	☐	☐	☐	☐
216	711/111 ; 711/121 ; 712/23 ; 712/29 ; 712/36		Popelka, Paul , et al.	☐	☐	☐	☐	☐	☐	☐
217	709/1		Thorson, Greg , et al.	☐	☐	☐	☐	☐	☐	☐
218	709/200 ; 709/213 ; 709/229 ; 710/243 ; 710/52 ; 711/100		VanDoren, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
219	711/141 ; 711/147 ; 711/149 ; 711/169		Tarui, Toshiaki , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
220	☒	☐	US 6088768 A	20000711		Method and system for maintaining cache coherence in a multiprocessor-multicache environment having unordered communication	711/141
221	☒	☐	US 6091857 A	20000718		System for producing a quantized signal	382/251
222	☒	☐	US 6094715 A	20000725		SIMD/MIMD processing synchronization	712/20
223	☒	☐	US 6094686 A	20000725		Multi-processor system for transferring data without incurring deadlock using hierarchical virtual channels	709/240
224	☒	☐	US 6101420 A	20000808		Method and apparatus for disambiguating change-to-dirty commands in a switch based multi-processing system with coarse directories	700/5
225	☒	☐	US 6101181 A	20000808		Virtual channel assignment in large torus systems	370/352

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
220	711/118 ; 711/119 ; 711/130		Baldus, Donald Francis , et al.	☐	☐	☐	☐	☐	☐	☐
221	341/200 ;		Shaw, Venson M. , et al.	☐	☐	☐	☐	☐	☐	☐
222	712/203		Wilkinson, Paul Amba , et al.	☐	☐	☐	☐	☐	☐	☐
223	709/236 ; 709/237 ; 709/238 ; 709/239 ; 710/29		Sharma, Madhumitra	☐	☐	☐	☐	☐	☐	☐
224	200/2 ; 200/3 ; 709/201 ; 709/215 ; 709/216 ; 712/28 ; 712/29 ; 712/32		VanDoren, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
225	709/238 ; 709/239 ; 709/240		Passint, Randal S. , et al.	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
226	☒	☐	US 6108752 A	20000822		Method and apparatus for delaying victim writes in a switch-based multi-processor system to maintain data coherency	711/117
227	☒	☐	US 6108340 A	20000822		Incidence graph based communications and operations method and apparatus for parallel processing architecture	370/406
228	☒	☐	US 6118392 A	20000912		Lossless data compression with low complexity	341/60
229	☒	☐	US 6118817 A	20000912		Digital video signal encoder and encoding method having adjustable quantization	375/240
230	☒	☐	US 6120298 A	20000919		Uniform motivation for multiple computer-assisted training systems	434/236
231	☒	☐	US 6121904 A	20000919		Lossless data compression with low complexity	341/65

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
226	710/131 ; 710/19 ; 710/21 ; 710/39 ; 710/52 ; 710/55 ; 710/59 ; 711/143 ; 711/144 ; 711/152 ; 711/156 ; 711/168		VanDoren, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
227			Rolfe, David B. , et al.	☐	☐	☐	☐	☐	☐	☐
228	341/65		Levine, Earl	☐	☐	☐	☐	☐	☐	☐
229			Wang, Albert S.	☐	☐	☐	☐	☐	☐	☐
230	434/118 ; 434/322 ; 434/323 ; 434/327 ; 434/335 ; 434/353 ; 434/362		Jenkins, William M. , et al.	☐	☐	☐	☐	☐	☐	☐
231	341/106		Levine, Earl	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
232	☒	☐	US 6122714 A	20000919		Order supporting mechanisms for use in a switch-based multi-processor system	711/150
233	☒	☐	US 6125348 A	20000926		Lossless data compression with low complexity	704/500

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
232	710/131 ; 711/121 ; 711/141 ; 711/149 ; 711/151		VanDoren, Stephen R. , et al.	☐	☐	☐	☐	☐	☐	☐
233	704/230 ; 704/501 ; 704/502 ; 704/503 ; 704/504		Levine, Earl	☐	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
1	☐	☐	US 5113523 A	19920512	64	High performance computer system	712/12
2	☐	☐	US 5305446 A	19940419	73	Processing devices with improved addressing capabilities, systems and methods	712/34
3	☐	☐	US 5410652 A	19950425	75	Data communication control by arbitrating for a data transfer control token with facilities for halting a data transfer by maintaining possession of the token	370/450
4	☐	☐	US 5535348 A	19960709	72	Block instruction	712/241
5	☐	☐	US 5594914 A	19970114	72	Method and apparatus for accessing multiple memory devices	712/42
6	☐	☐	US 5751991 A	19980512	64	Processing devices with improved addressing capabilities, systems and methods	711/214
7	☐	☐	US 5809309 A	19980915	64	Processing devices with look-ahead instruction systems and methods	710/260
8	☐	☐	US 5826101 A	19981020	68	Data processing device having split-mode DMA channel	712/34

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1			Colley, Stephen R. , et al.	☒	☐	☐	☐	☐	☐	☐
2			Leach, Jerald G. , et al.	☒	☐	☐	☐	☐	☐	☐
3	370/455 ; 370/457 ; 370/462 ; 710/240		Leach, Jerald G. , et al.	☒	☐	☐	☐	☐	☐	☐
4			Leach, Jerald G. , et al.	☒	☐	☐	☐	☐	☐	☐
5			Coomes, Joseph A. , et al.	☒	☐	☐	☐	☐	☐	☐
6	711/220 ; 712/208		Leach, Jerald G. , et al.	☒	☐	☐	☐	☐	☐	☐
7	712/233		Leach, Jerald G. , et al.	☒	☐	☐	☐	☐	☐	☐
8	710/22		Beck, Michael D. , et al.	☒	☐	☐	☐	☐	☐	☐

	U	1	Document ID	Issue Date	Pages	Title	Current OR
9	☐	☐	US 5937202 A	19990810	219	High-speed, parallel, processor architecture for front-end electronics, based on a single type of ASIC, and method use thereof	712/19

	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3	4	5
9	712/11		Crosetto, Dario B.	☒	☐	☐	☐	☐	☐	☐

	Document ID	Kind Codes	Source	Issue Date	Pages
1	US 5113523 A		USPAT	19920512	64
2	US 5305446 A		USPAT	19940419	73
3	US 5410652 A		USPAT	19950425	75
4	US 5535348 A		USPAT	19960709	72
5	US 5594914 A		USPAT	19970114	72
6	US 5751991 A		USPAT	19980512	64
7	US 5809309 A		USPAT	19980915	64
8	US 5826101 A		USPAT	19981020	68

	Title	Abstract	Current OR
1	High performance computer system		712/12
2	Processing devices with improved addressing capabilities, systems and methods		712/34
3	Data communication control by arbitrating for a data transfer control token with facilities for halting a data transfer by maintaining possession of the token		370/450
4	Block instruction		712/241
5	Method and apparatus for accessing multiple memory devices		712/42
6	Processing devices with improved addressing capabilities, systems and methods		711/214
7	Processing devices with look-ahead instruction systems and methods		710/260
8	Data processing device having split-mode DMA channel		712/34

	Retrieval Classif	Current XRef	Inventor	U	S	C	P	1	2	3	4	5
1			Colley, Stephen R. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐
2			Leach, Jerald G. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐
3		370/455 ; 370/457 ; 370/462 ; 710/240	Leach, Jerald G. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐
4			Leach, Jerald G. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐
5			Coomes, Joseph A. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐
6		711/220 ; 712/208	Leach, Jerald G. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐
7		712/233	Leach, Jerald G. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐
8		710/22	Beck, Michael D. , et al.	☐	☒	☐	☐	☐	☐	☐	☐	☐

	Document ID	Kind Codes	Source	Issue Date	Pages
9	US 5937202 A		USPAT	19990810	219

	Title	Abstract	Current OR
9	High-speed, parallel, processor architecture for front-end electronics, based on a single type of ASIC, and method use thereof		712/19

	Retrieval Classif	Current XRef	Inventor	U	S	C	P	1	2	3	4	5
9		712/11	Crosetto, Dario B.	☐	☒	☐	☐	☐	☐	☐	☐	☐